SENSE AMPLIFIER FOR MEMORY DEVICE

ABSTRACT

A memory charging circuit includes a read charge control circuit controlled according to a read control signal and an address value. A write charge control circuit is controlled according to a write control signal and the same or a different address value. Charging to and charging from the same data IO lines is controlled using the read charge amplifier circuit and the write charge amplifier circuit. A column select line circuit can be configured into a first arrangement where a first output is activated according to a read control signal and an address and a second output is activated according to a write control signal and the same or a different address. In a second arrangement, the first output is activated according to an address and either the read control signal or the write control signal.